

Eric LESCOUET, *et al.*  
Serial No. 10/573,881  
March 14, 2011

**AMENDMENTS TO THE DRAWINGS:**

Applicants submit concurrently herewith ten (10) replacement sheets of drawings illustrating Figs. 1, 2a, 2b, 3-8, 9a, 9b and 10-13 in compliance with 37 C.F.R. §§1.84 and 1.121(d).

Attachments: Replacement Sheets (10)

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### **REMARKS/ARGUMENTS**

Reconsideration of this application is respectfully requested.

In response to the formality-based drawing objections, reference signs not found in the drawings have now been deleted from the written text of the specification – and a complete new set of more legible replacement drawings are concurrently submitted herewith.

As requested, the related application paragraph has been updated with the current status of applications reference therein.

As requested, the few instances of acronyms that do not already first include a description in plain text have been amended so as to do so.

Similarly, in response to the objection due to imbedded hyperlinks or other forms of browser-executable code, such have been deleted by the above amendments.

In response to the formality-based objections to claim 33, this claim has also been amended so as to moot the Examiner's stated ground for objection.

The provisional double-patenting rejections *vis-à-vis* copending related application Serial Nos. 10/552,608 and 10/573,881 are noted. However, since the final form of claims to be allowed in these applications has not yet been determined and/or because of the above amendments to the claims in this present application, no further action at this time is believed to be required.

In response to the rejection of claims 30 and 31 under 35 U.S.C. §101, claim 30 has been amended in accordance with the Examiner's helpful suggestions and claim 31 has been cancelled.

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With respect to the rejection of claims 35 and 36 under 35 U.S.C. §112, second paragraph, these claims have been amended so as to obviate the Examiner's stated grounds for rejection.

The rejection of claims 1-5, 9-20, 23 and 25-35 under 35 U.S.C. §102 as allegedly anticipated by Ohno '016, the rejection of claims 6-8 and 21-22 under 35 U.S.C. §103 as allegedly being made "obvious" based on Ohno '016 in view of Endo '303, the rejection of claim 36 under 35 U.S.C. §103 as allegedly being made "obvious" based on Ohno in view of Kahle '823, and the rejection of claim 24 under 35 U.S.C. §103 as allegedly being made "obvious" based on Ohno in view of Endo and in further view of Songer '327 are all respectfully traversed.

Claim 1 now includes features from previous claims 2, 4 and 7. In addition, claim 1 recites the feature that the third memory context is used as an intermediate address space when the common program is invoked by the second operating system. This amendment finds basis in the second paragraph of the original specification at page 31. Independent claims 33 and 35 have been similarly amended.

The cited prior art does not disclose or suggest the combination of features recited by the amended independent claims. The amended independent claims now more clearly define how to switch between different memory contexts when invoking the common program.

When the common program is invoked by the first operating system, the current memory context **remains** the first memory context. In other words, the first operating system and the common program **share the same memory context**.

In contrast, when the common program is invoked by the second operating system, the current memory context is changed to the third memory context (i.e., the memory context associated with the common program). Thereby, the third memory

context is used as an intermediate address space when switching from the second to the first memory contexts.

By having the first operating system and the common program share the same memory context, switching of memory contexts can be avoided when transitioning to/from the first operating system, thereby enabling the first operating system to run with minimum overhead.

On the other hand, by providing a third memory context associated with the common program and using that context as an intermediate address space, it becomes possible to switch from the second operating system to the first operating system (and *vice versa*) on an architecture such as the IA-32 Intel architecture. More particularly, by implementing a (MMU) context switch as recited by the new independent claims, it becomes possible to run multiple independent operating systems concurrently on a single CPU such as an Intel IA-32 CPU.

In other words, the present invention is based on an asymmetric architecture that uses  $N+1$  (e.g., three) memory contexts for switching between  $N$  (e.g., two) operating systems.

The cited prior art does not disclose or suggest these features.

Ohno does not disclose or suggest an asymmetric architecture wherein first and second operating system are associated with first and second memory contexts, respectively, and a common program is associated with a third memory context, wherein the first operating system and the common program share the first memory context so that invoking the common program by the first operating system does not require switching the memory context switch, whereas invoking the common program by the second operating system results in switching from the second to the third memory context as an intermediate memory context.

Moreover, Ohno's "inter-OS control program" appears to be part of both OS-A and OS-B memory contexts, i.e., its code and data are mapped in both page tables (see, e.g., FIG. 2 in Ohno). That means that the "control program" is part of the so called "shared memory space". Thereby the control program can be executed from both OS contexts when an interrupt occurs or to have function calls to/from OS-A or OS-B. In other words, Ohno discloses only two memory contexts.

In contrast, according to the presently claimed invention, the "common program" has its own memory context that maps the KV (kernel one-to-one) mapping of the second (and every possible additional guest) operating system. In addition, the common program is part of the first memory context; thus, the common program can execute either in the first memory context or in its own (the third) memory context while switching to/from the second operating system.

In summary, the present invention is distinguished from Ohno at least based on the following features:

- there are  $N+1$  memory contexts (for  $N$  operating systems)
- the common program is not part of the memory context of the second operating system
- there is no direct function call between the second operating system and the common program
- switching to/from the second operating system is done via CPU hardware mechanism (e.g., Intel IA32 task switch) that allows switching from the second context (memory and registers) to the common program (third) memory context
- the common program context is used as an intermediate context when switching between the first and second operating systems.

Similar considerations apply to Endo, who discloses that when switching from the general purpose OS to the real time OS, the value of the register being used is temporarily stored in the storage context 157 for the general purpose OS (see, e.g., 9:53-56). Conversely, when switching from the real time OS to the general purpose OS, the value of the register being used is temporarily stored in the storage context for the real time OS (see, e.g., 9:60-63). Accordingly, Endo does not disclose a common program having its own (third) memory context. In any case, Endo does not disclose or suggest an asymmetric architecture wherein first and second operating systems are associated with first and second memory contexts, respectively, and a common program is associated with a third memory context, wherein the first operating system and the common program share the first memory context so that invoking the common program by the first operating system does not require switching the memory context, whereas invoking the common program by the second operating system results in switching from the second to the third memory context as an intermediate memory context.

Accordingly, the present claims are believed to patentably define over Ohno and Endo taken singly or in combination. Since Kahle and Songer do not solve the deficiencies of Ohno and Endo discussed above, the present claims patentably define over all of the cited prior art taken singly or in any combination.

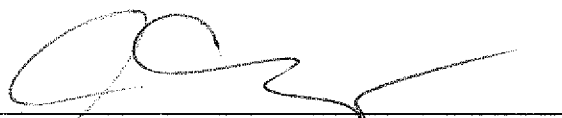
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Accordingly, this entire application is now believed to be in condition for allowance, and a formal notice to that effect is earnestly solicited.

Respectfully submitted,

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